**Memory Numericals**

1 KB= 1024 Bytes = 210

MB= 220

GB = 230

**Q.1 a) How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?**

**b) How many lines of the address bus must be used to access 2048 bytes of memory?**

**c) How many of these lines will be common to all chips?**

Solution: a) 128 x 8 RAM means the Storage capacity of 1024 bits  
 and     
                          1 byte= 8bits

1 bit = 0.125 Byte

Thus,                1024 bits = 1024 \* 0.125  
                                         = 128 Byte  
That means that 1 RAM chip has the storage capacity of 128 Byte  
   Lets consider there are n number of Chips to provide 2048 Bytes  
 Now,  
                                  1 RAM Chip = 128 Byte  
Thus,                          N RAM Chips = 2048 Bytes           
   
      Cross Multiplying the equations  
                                     128 \* n = 2048             
  
Thus,                              n = 2048/128 =16 chips.

b) 2048 = (2 power 11) = 11 address lines are needed to address 2048 bytes.

c) 128 = (2 power 7) = 7 lines to address the chip.

Practice: a) [How many 64 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?](https://gateoverflow.in/83365/many-ram-chips-are-needed-provide-memory-capacity-2048-bytes)

b) How many lines of the address bus must be used to access 4096 bytes of memory?

**Q.2 How many 128×8 bit RAMs are required to design 32K×32 bit RAM?**

Number of RAM = (32 \* K \* 32) / 128 \* 8   
  
                       = 25 \* 210 \* 25   /  27 \* 23   
  
                       =220 / 210   
  
                        = 1024 RAMS

**Q.3 A cache memory needs an access time of 30 ns and main memory 150 ns, what is average access time of CPU (assume hit ratio = 80%)?**

**Effective Memory Access Time = (Cache hit x Cache access time) + (Cache miss x (Cache miss Penalty + memory Access time))**

cache hit=0.8, cache access time=30ns

cache miss= 1-0.8= 0.2

 = 0.8(30) + 0.2(30+150) ns  
  
 = 24 + 0.2(180) ns  
  
 = 24 + 36 ns = 60 ns.

**Practice: A cache memory needs an access time of 50 ns and main memory 200 ns, what is average access time of CPU (assume hit ratio = 70%)?**

**Q.4 A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.**

**i) How many bits are there in the tag, index, block, and word fields of the address format?**

**ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.**

Solution: i) Main memory has 64K = 64 x 1024 = 2^6 x 2^10 = 2^16 words = 16 address line  
Cache memory has 1K = 1024 = 2^10 words = 10 address line

**MM= Tag + Index**

**16 = tag + 10**

**Tag= 16-10= 6**  
  
Cached address consists of Index and Tag part. Index and Tag together make main memory address.

Index part addresses cache memory and Tag part represents the rest of the main memory address.  
In this case to address main memory we need 16 bits (2^16) and to address cache memory we need 10 bits (2^10).

So Index is 10 bits wide and Tag is 6 bits wide (16 - 10 = 6).  
  
When using blocks the Index is divided into the "Block" part and the "Word" part. Block part addresses blocks of cache memory and Word part addresses individual words in a block.  
In this case the block is **4 words long** for what we need 2 bits (2^2) and that leaves 8 bits (10 - 2 = 8) for addressing blocks.  
Summary:  
Tag = 6 bits  
Index = 10 bits  
Block = 10-2= 8 bits  
Word = 2 bits  
  
ii) For the above example a cache word with a Valid bit would contain

6Tag 8block 2word

6 Tag 10 Index

  
Valid bit = 1 bit  
Tag = 6 bits  
Data = 16 bits  
total bits = 1+6+16= 23 bits